What is claimed is:

1. A method of fabricating an MIM capacitor of high capacitance in a semiconductor device, the method comprising:

depositing an interlayer dielectric film on a metal line;

etching the interlayer dielectric film to form an MIM capacitor forming region;

sequentially depositing a lower electrode layer, an insulator layer and an upper electrode layer on the interlayer dielectric film; and

etching the lower electrode layer, the insulator layer and the upper electrode layer to form an MIM capacitor.

2. A method as defined by claim 1, wherein a capacitance of the MIM capacitor is determined by controlling a thickness of the interlayer dielectric film.

3. A method as defined by claim 1, wherein the interlayer dielectric film is made of USG or TEOS.

4. A method as defined by claim 1, wherein the lower electrode layer is made of Ti, W or TiN.

5. A method as defined by claim 1, wherein the insulator layer is made of TaO_2, Al_2O_3 or SiN.

6. A method as defined by claim 1, wherein the upper electrode layer is made of Ru, Pt or TiN.

7. A method of fabricating an MIM capacitor of high capacitance in a semiconductor device, the method comprising:

depositing an interlayer dielectric film on a metal line;

planarizing the interlayer dielectric film;

etching the interlayer dielectric film to form an MIM capacitor forming region;

sequentially depositing a lower electrode layer, an insulator layer and an upper electrode layer on the interlayer dielectric film; and

planarizing the lower electrode layer, the insulator layer and the upper electrode layer to form an MIM capacitor.

8. A method as defined by claim 7, wherein a capacitance of the MIM capacitor is determined by controlling a thickness of the interlayer dielectric film.

9. A method as defined by claim 7, wherein the interlayer dielectric film is planarized by a chemical mechanical polishing (CMP) process.

10. A method as defined by claim 7, wherein the interlayer dielectric film is planarized by an etch-back process.

11. A method as defined by claim 7, wherein the lower electrode layer is made of any one of Ti, W or TiN.

12. A method as defined by claim 7, wherein the insulator layer is made of any one of TaO_2, Al_2O_3 or SiN.

13. A method as defined by claim 7, wherein the upper electrode layer is made of any one of Ru, Pt or TiN.

14. A method as defined by claim 7, wherein the lower electrode layer, the insulator layer and the upper electrode layer are planarized by a chemical mechanical polishing (CMP) process.

15. A method as defined by claim 7, wherein the lower electrode layer, the insulator layer and the upper electrode layer are planarized by an etch-back process.